DESIGN OF A 4.4 TO 5 GHz LNA IN 0.25-µm SiGe BiCMOS TECHNOLOGY

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ABSTRACT
This paper describes a Low-Noise Amplifier (LNA), designed using a 0.25-µm SiGe process, operating in the 4.4–5 GHz band. A power gain of 12.8 dB at 5 GHz has been achieved with a power consumption of 23.77 mW using a 2 V power supply. The noise figure is 2.2 dB while the input referred 1dB compression point is −6.2 dBm.

1. INTRODUCTION
The huge, fast growth of the wireless communication market has caused an ever-increasing demand for front-end RF circuits; their low-cost requirements cannot be satisfied by discrete circuits, forcing the use of monolithic integrated circuits [1–3]. The required performances are steadily increasing as the demand for more communication bandwidth forces the use of higher and higher frequency bands.

Bipolar transistors are usually preferred, for optimal performance, to MOSFET implementations. The silicon–germanium (SiGe) BiCMOS process is one of the most promising technologies that should replace the expensive composite semiconductors (such as GaAs, InP, and so on) while maintaining comparable performances, thanks to the high performances of the n-p-n SiGe-based bipolar transistors, and the possibility of large scale integration typical of the Si IC technology [4]. The technology used also offers lateral and vertical p-n-p bipolar transistors, 1.4-kΩ/□ and 50-Ω/□ resistors, varactor diodes, electrostatic discharge diodes (ESD), MIM and MOS capacitors, and MOS transistors with minimum channel length of 0.25 µm.

The Low-Noise Amplifier (LNA) is a fundamental block of analog communication systems, especially for wireless communication. This work presents an LNA, designed for a 0.25-µm SiGe IC process, that operates in the 4.4 GHz to 5 GHz frequency range.

2. DESIGN AND OPTIMIZATION
The design of an LNA involves many trade-offs to meet the performance specifications. Good linearity may be achieved using large transistors, high DC current, and eventually a feedback network. Nevertheless the feedback limits the maximum gain while a sufficiently low noise figure requires a moderate current.

The common-emitter configuration seems the best choice to satisfy both the gain and noise figure requirements by trading off noise figure for gain when choosing the bias current. A good linearity can be achieved by the use of big transistors, a sufficiently high current (which also provides a sufficient gain) and an inductive feedback network. Fig. 1 shows the schematic of the LNA.

The heterojunction bipolar transistor (HBT) Q0 amplifies the signal, while Q2 is used to bias Q0 by means of base current injection, thus avoiding the reduction of output voltage swing caused by the use of a resistive self-biasing configuration. The capacitors C0 and C1 are used to get an AC coupling of the stage. The inductors L0, L1 (L2) are used to match the input (output) impedance to 50 Ω. L1 and L2 are also used to maximize the dynamic range of the output. The resistances R0, R2, R3, and R4 cooperate with Q2...
to generate the bias base current of Q0, while the capacitor C3 decouples Q0 from the bias circuit (with the exception of R0, that must have a high resistance value to reduce its influence in Q0 and in the impedance matching) at the operating frequencies. A low noise figure has been achieved by using only reactive elements, i.e. capacitors and inductors; no emitter and/or collector resistors are used, as they impact not only the noise figure but also the maximum voltage swing, reducing the linearity.

The voltage drops on the junctions of HBT Q0 can be higher than the signal voltage swing during a fraction of the signal period; this might cause their associated parasitic diodes to breakdown or to work in the low-impedance operating region. A low (2 V) voltage supply has been used to prevent the voltage drops from being large enough to cause breakdown or direct-mode bias of the diodes. In general the results of simulations are not in satisfying agreement with the performances predicted by hand-written equations, so we had often to use numerical optimizations.

The first design step consisted in the choice of the width and of the bias current of the HBT Q0: a good compromise between gain and noise figure is achieved by using a transistor with a $2 \times 20 \mu m$ emitter, biased by a collector current of 10.9 mA. However the simple Common Emitter configuration does not exhibit a sufficient linearity. This can be improved with a feedback network provided by the emitter inductor L1, introduced also in order to improve the input matching.

In the next step, the input-output matching is achieved by setting the inductors values. Since the intrinsic capacitance $C_{\mu}$ couples the input and the output, it introduces a real part in the amplifier output impedance, whose value also depends on the HBT input impedance and on the input matching inductances. So it is possible to choose the input inductances so that the LNA input impedance is 50 $\Omega$ and the real part of the output impedance is about 50 $\Omega$. This solves the problem of matching the real part of the output impedance – a result which cannot be reached by using the output resistance of the transistor as it is quite too high for this task. As a consequence, we can avoid the use of a collector integrated resistor for the output matching, allowing us to match the imaginary part of the output impedance to zero by using the inductor L2. The above component values obtained analytically have been used as starting point for a numerical optimization in order to obtain a performance-driven design centering at schematic level.

2.1. Design at the layout level

The technology used supports many passive components such as resistors, capacitors, and inductors. In the LNA design the inductors are the most critical devices; they use only the wider, thicker metal layer (metal 5) which has also the lowest capacitive coupling to the $p$-well. There are different inductor types: some of them are designed to be used in a differential configuration, others are optimized for low inductance values, other types can be used to obtain high inductance values. All the inductor types share a patterned ground shield, used to minimize the currents induced into the $p$-well by the inductor. External shields are also included in the inductor type used in this design to avoid any coupling between the inductor and the adjacent circuits. All the capacitors are MIM capacitors, as they have a good linearity and they have few parasitics, especially if compared to the MOS capacitors.

Many iterations have been performed to minimize the layout vs. schematic performance loss caused by the layout parasitics. The floorplanning of the components was optimized to keep the critical paths short. Only the upper metal layers (metal4 and metal5) were used for the critical interconnects. In this way the Q0 base-bias circuit connection does not introduce a significant capacitive ground coupling. To lower the resistance of the connections of the high-current terminals of Q0 (the emitter and the collector) and the inductors, extra metal layers have been put on top of the metal layers (metal1 and metal2) included in the standard bipolar layout. These extra metal paths should also limit the density of the current flowing through the terminals of Q0. Only shielded inductors were used, in order to prevent parasitics’ effects at very high frequencies. The substrate electromagnetic behavior has been analyzed by using Momentum, a 2-D electromagnetic simulator, to detect the effects of the nonzero impedance between the upper face of the $p$-well and ground. In the technology used in fact the substrate and the $p$-well are separate silicon structures: the substrate is the basic $p$-doped silicon wafer, placed onto the ground plane; the $p$-well is placed onto the substrate and is much thinner than the substrate.

More in detail, the non-ideal behavior of the $p$-well has been investigated by analyzing the equivalent circuit of some transmission lines in which the upper conductor is a metal
line, the lower conductor is the ground plane and the space between them is filled by the $p$-well and by the substrate. In different simulations, the $p$-well is connected to ground by using contacts (to a metal line kept at ground voltage) with variable position and distance. The transmission lines don’t have the same behavior of an ideal line with the $p$-well replaced by an ideal conductor. The non-ideality of the $p$-well can be accounted for by placing a parallel RC circuit between the connections and ground; the resistance and the capacitance values depend both on the metal used to build the transmission line and on the number and position of the contacts. This did not seem to affect the behavior of our circuit, as a higher impedance to ground in series to the signal-to-substrate parasitics lowers the signal-to-ground coupling.

The proper sizing of the inductors is critical for good performance; their nonideality was the main reason of the poor matching between the analytically predicted performances (where the optimal inductor sizes are determined on the basis of an approximate analytical circuit model) and the simulated ones. The quality factor for one of the inductors used in our design (the collector inductor) has been computed in order to quantify the non-ideality of the available inductors; at 4.7 GHz it is about 10.5, as can be seen in Fig. 2.

As a final step the pad effects have been considered and investigated. At the layout level the pads introduce large parasitic capacitances, extracted by using DIVA: the post-layout simulation has shown significant performance degradation, even in absence of the ESD diodes, due to signal-to-ground coupling. To limit this coupling, the metal shield between the pad plate and the substrate has been connected to ground by a 10 kΩ resistor. All the layout parasitics modify the performances and require re-optimizing all the component values, especially the values of the capacitances and of the inductances. The final layout is depicted in Fig. 3.

3. PERFORMANCES

The results of the post-layout simulations including the effects of the pads and of the layout-associated parasitics are shown in Figs. 4–6. Figure 4 shows the gain of the LNA, that varies of about 1 dB in the working bandwidth, as the operating frequency is well beyond the corner frequency of the HBT. In absence of zeroes flattening the harmonic response of the device (requiring some extra passive devices), gain varies as $1/f$. This issue, in conjunction with the need of reaching an adequate noise figure level, has caused a decrease of the gain especially at the higher frequencies. On the other hand, the cascode configuration cannot be used as a single-stage LNA design option when a high linearity is required, especially if a relatively low voltage supply is adopted.

In Fig. 5 the input and the output reflection coefficients are reported as function of frequency. In the 4.4–5 GHz operating frequency range, the $S_{11}$ is considerably better than the $S_{22}$. This can be explained by noting that the input and the output impedances of the LNA cannot be fixed independently one of each other: they are coupled because of the effect of $C_{ij}$. So, when we managed to match the input impedance to 50 Ω, the resulting real part of the output impedance did not match exactly 50 Ω; this has determined the output impedance mismatch, even in presence of a good matching of the output reactance to zero. The input referred compression point ($P_{I1dB}$) at 4.7 GHz is of $-6.2$ dBm and
the input referred third-order intercept point (IIP3) is of 11.6 dBm. Figure 6 reports the noise figure (NF).

Table 1 summarizes the layout-level corner values of the achieved performances, in the 4.4–5 GHz working frequency range.

4. Conclusion

A single-stage LNA has been designed in a 0.25-µm 1-poly 5-metal SiGe BiCMOS/RFCMOS technology. The operating frequency range is 4.4–5 GHz. The amplifier achieves a power gain of 12.8 dB at 5 GHz, a NF of 2.2 dB, a $P_{I1dB}$ of $-6.2$ dBm at 4.7 GHz, and consumes 23.77 mW using a 2 V power supply. Input and output return loss are 13.8 dB and 8.46 dB, respectively.

5. References


